REMARKS

The Applicants request reconsideration of the rejection.

Claims 1-11 remain pending.

Claims 1-2, and 5-9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Baldwin et al., U.S. 6,735,422 (Baldwin) in view of Mo et al., U.S. Pat. Pub. 2004/219884 (Mo). The Applicants traverse as follows.

At the outset, the Applicants note that Mo has not been established as prior art to the present claims. Mo was filed in the United States on February 6, 2004, subsequent to the U.S. filing date of August 6, 2003 of the present application. The Applicants note Mo's claim to provisional application No. 60/445,525, filed on February 7, 2003. However, the teaching for which Mo, in combination with Baldwin, allegedly renders the claims unpatentable, is not found in the provisional application. Therefore, Mo is in fact only applicable as of its February 6, 2004, date, and thus the combination rejection fails to raise a prima facie case of unpatentablility.

The primary reference to Baldwin describes a system which has two loops: an AGC loop and a DC loop. In addition, Baldwin discloses various look-up tables which are populated with data during a calibration procedure. The calibration procedure is performed periodically. The description mentions

the term reduce DC offset. Thus, the DC loop tries to minimize the DC offsets at the receiver, and apparently the AGC loop acts to ensure that the "wanted" signal has the correct voltage swing at the baseband ADC input 313.

Mo is seen to describe a system that aims to improve the match between the I and Q receive channels in a receiver. To this end, Mo employs a radio transmitter 32 to generate a predetermined test signal, which passes to the radio receiver through the I and Q receive paths, is digitized by two ADCs, and fed to a baseband processor. The baseband processor controls a sequence of tests and, on the basis of the data collected from the two ADCs, makes corrections in the receiver to improve the receiver I-Q amplitude and phase match.

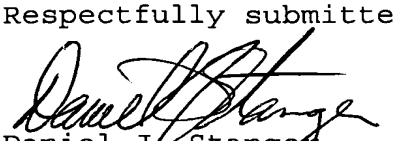
Thus, like Baldwin, Mo does not address the issue of optimizing the voltage levels at the interface between the radio receiver and the baseband ADC. Such optimization is necessary if the system is to use the full dynamic range of the baseband ADC converter and achieve Mo's stated objectives.

Therefore, in combination, Baldwin and Mo fail to disclose a semiconductor integrated circuit device for RF processing which frequency-converts a received signal into a baseband to output the signal as an I signal and a Q signal, comprising an external input terminal to which an adjustment

signal, giving instructions to adjust output-voltage levels of the I signal and Q signal, is input. The combination further fails to disclose or suggest an output-voltage adjustment unit as claimed in Claim 2, an amplifier for adjusting the output voltage levels of the I signal and Q signal based on a reference voltage input via the external input terminal as claimed in Claim 5, a comparison unit for preparing the digital data output from the ADC and a reference voltage, and for outputting the comparison results as an adjustment signal as claimed in Claim 7, a portable terminal system comprising first and second semiconductor integrated circuit devices as claimed in Claim 8, or the output-voltage adjustment unit, ADC, and comparison unit as claimed in Claim 9.

In view of the foregoing amendments and remarks, the Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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